FIG. 1

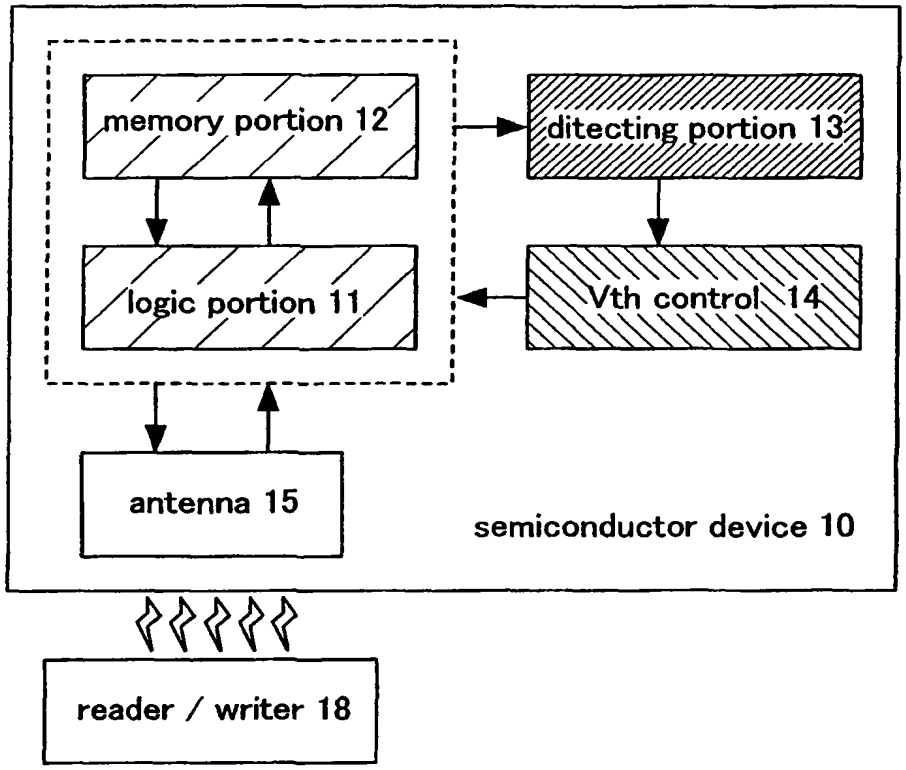

memory portion 12
ditecting portion 13
logic portion 11
Vth control 14
antenna 15
semiconductor device 10
reader / writer 18

FIG. 2A

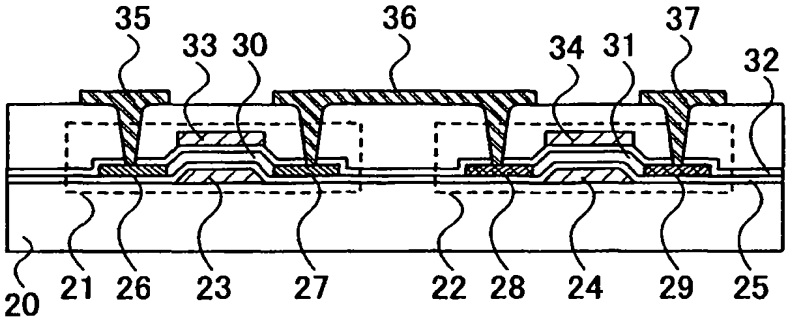


FIG. 2B

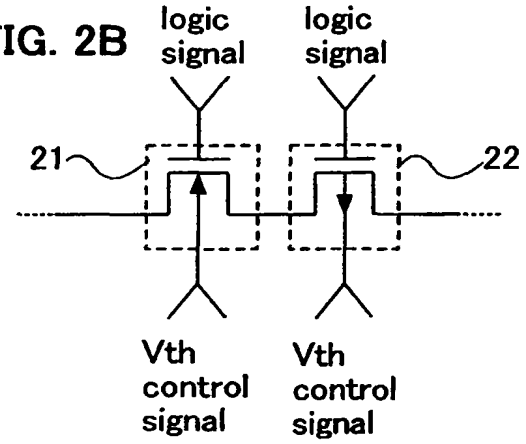


FIG. 2C

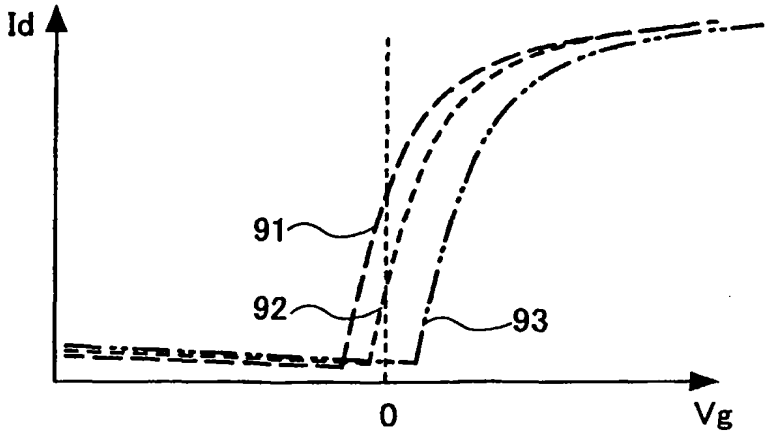


FIG. 3

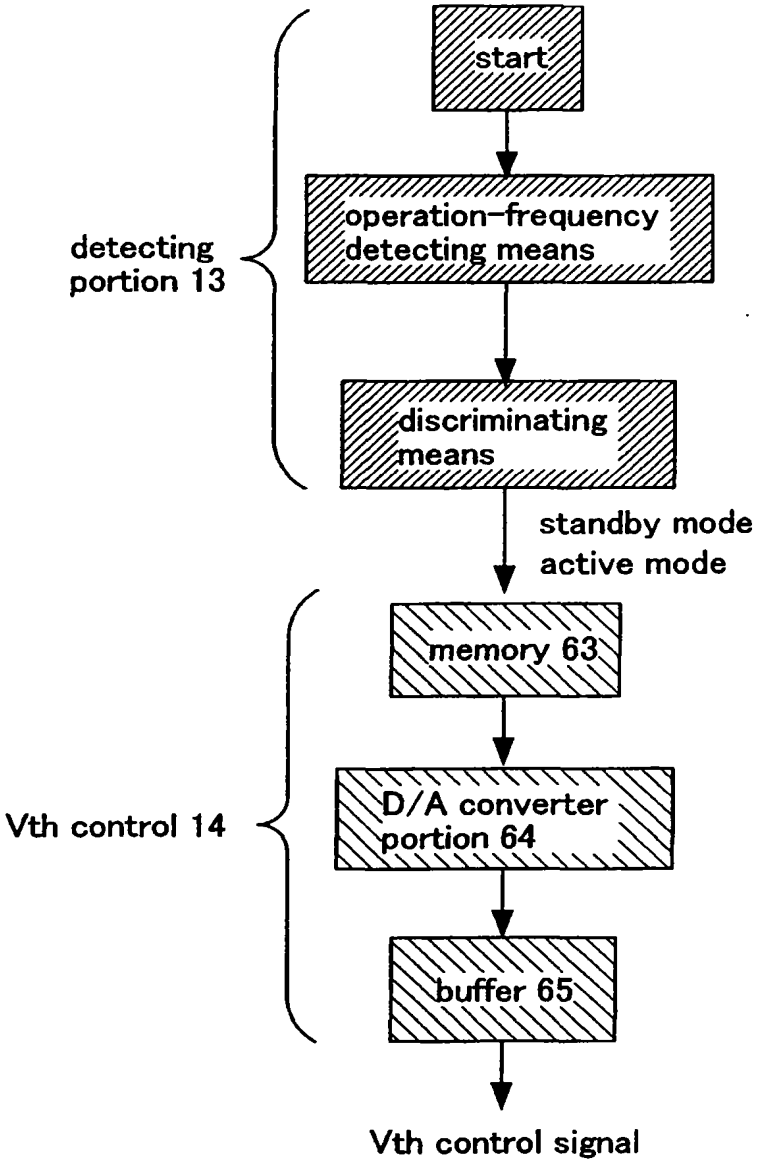

start
operation-frequency detecting means
detecting portion 13
discriminating means
standby mode
active mode
memory 63
D/A converter portion 64
Vth control 14
buffer 65
Vth control signal

FIG. 4A

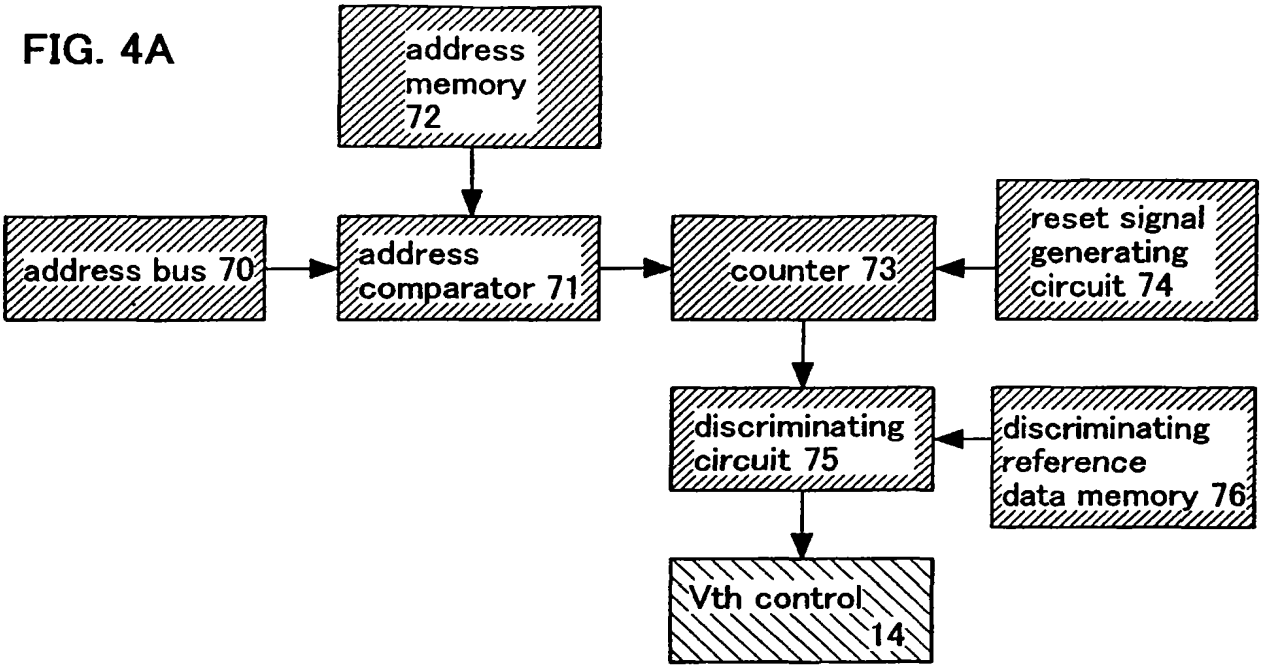
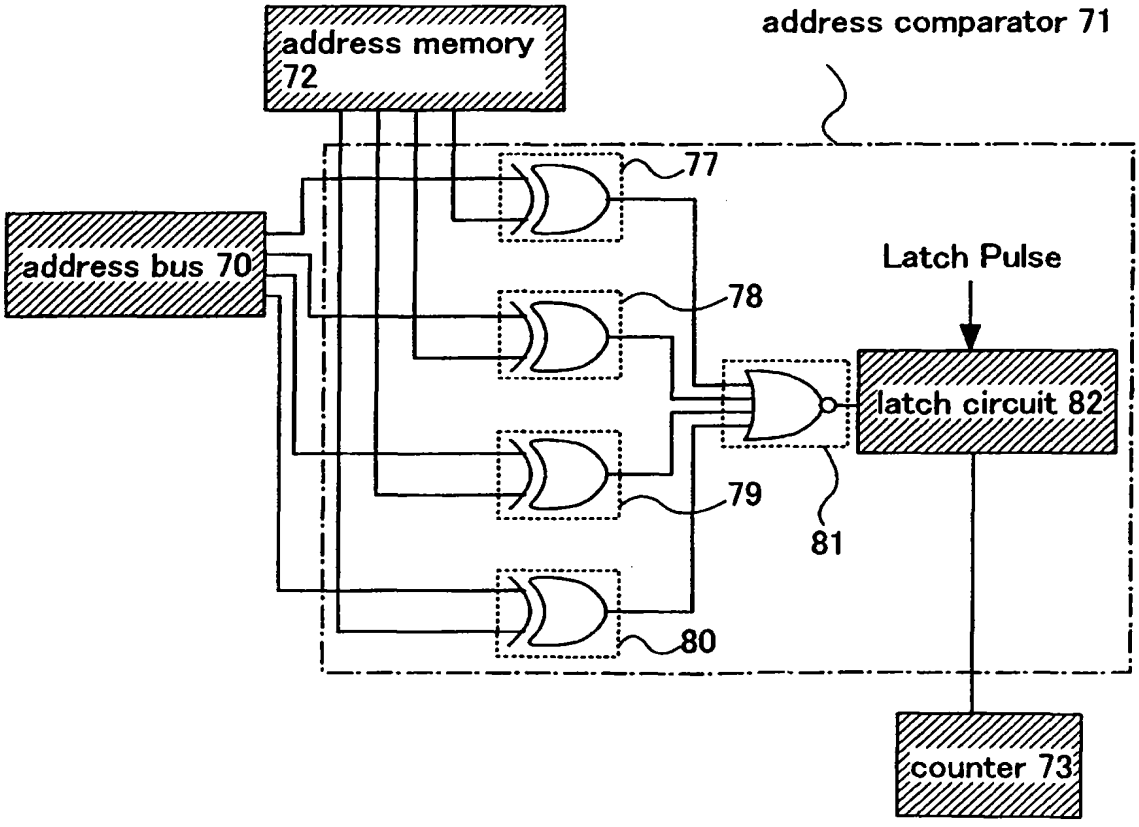

address memory 72
address bus 70
address comparator 71
counter 73
reset signal generating circuit 74
discriminating circuit 75
discriminating reference data memory 76
Vth control 14

FIG. 4B


address memory 72
address comparator 71
77
address bus 70
Latch Pulse
78
latch circuit 82
79
81
80
counter 73

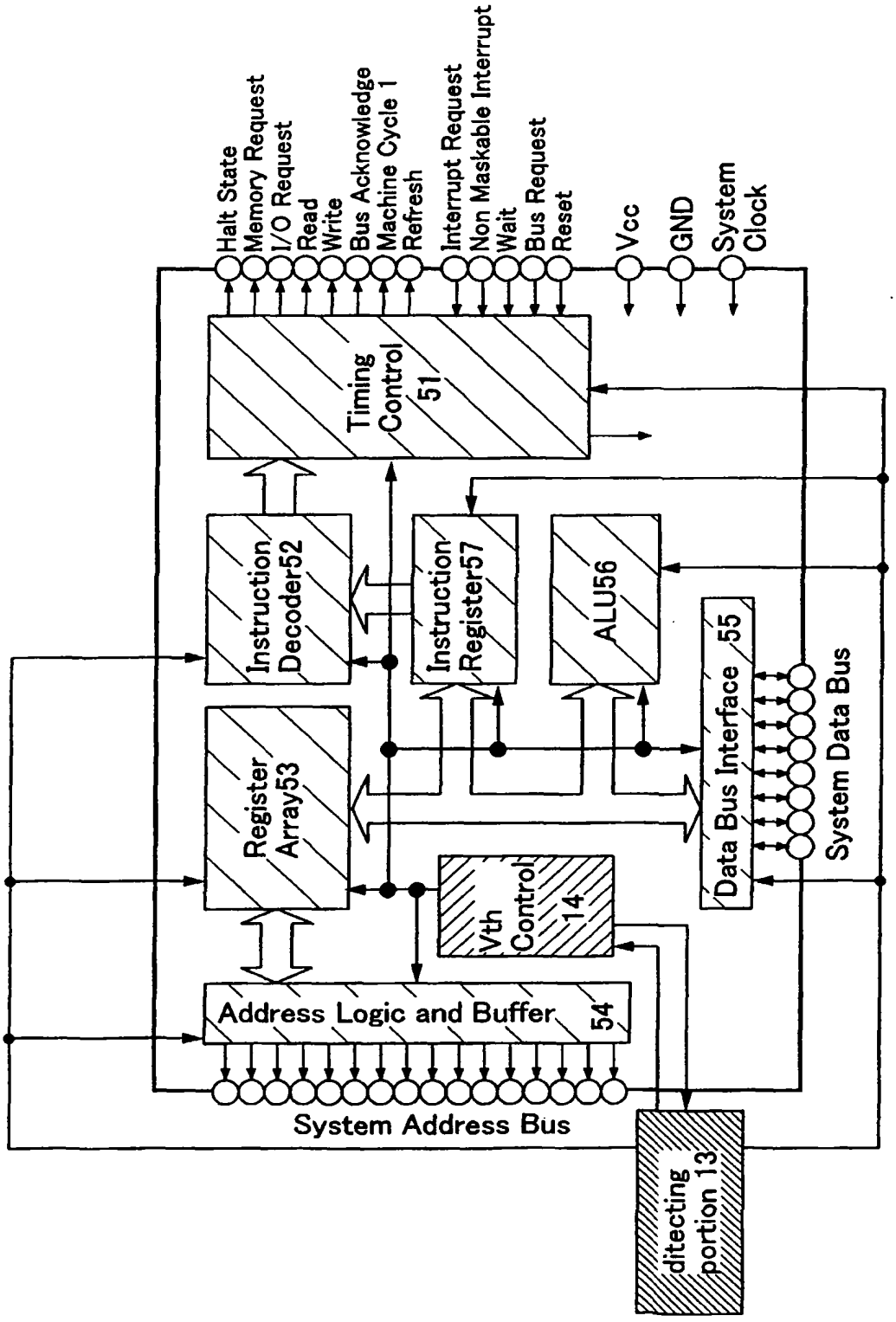

Halt State
Memory Request
I/O Request
Read
Write
Bus Acknowledge
Machine Cycle 1
Refresh
Interrupt Request
Non Maskable Interrupt
Wait
Bus Request
Reset
Vcc
GND
System Clock
Timing Control 51
Instruction Decoder52
Instruction Register57
ALU56
Register Array53
Data Bus Interface 55
System Data Bus
Vth Control 14
Address Logic and Buffer 54
System Address Bus
ditecting portion 13

FIG. 5

FIG. 6A

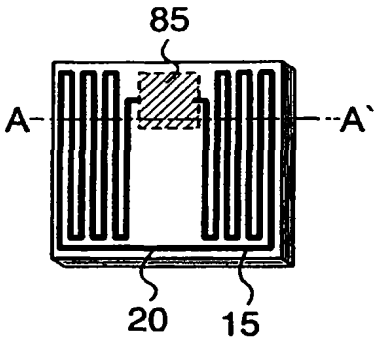


FIG. 6B

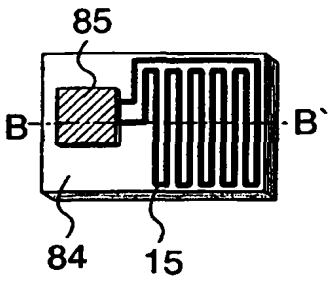


FIG. 6C

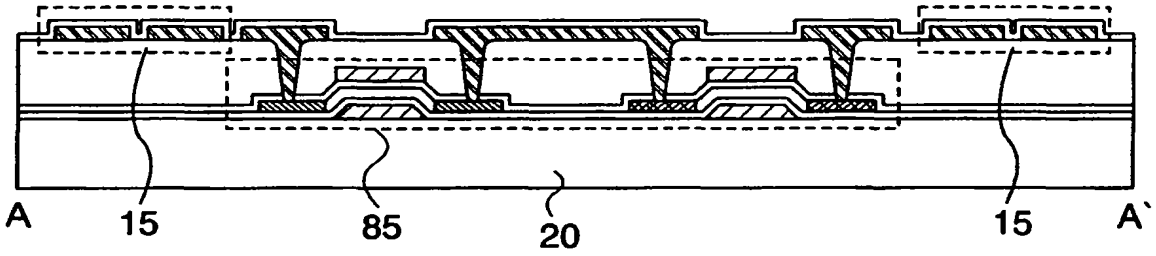


FIG. 6D

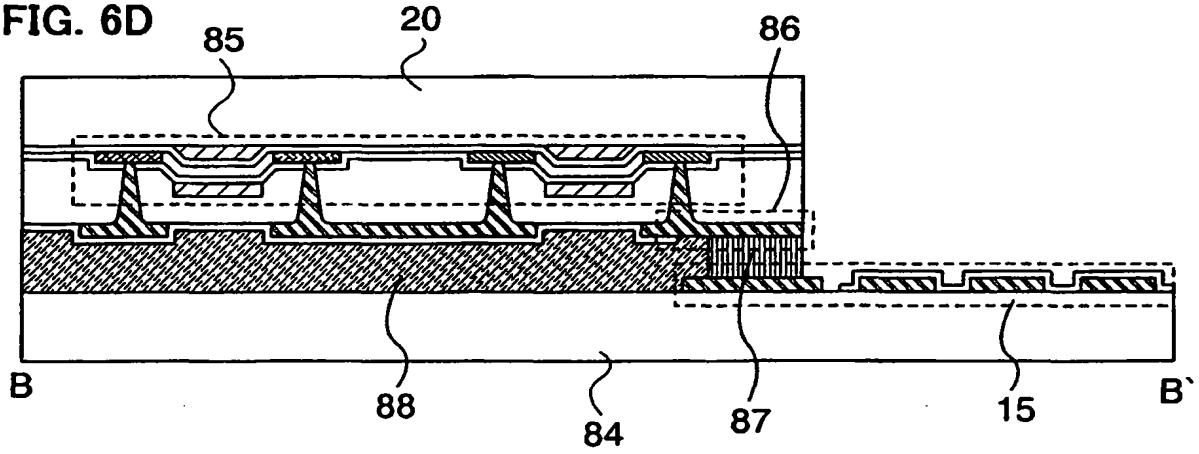


FIG. 7A

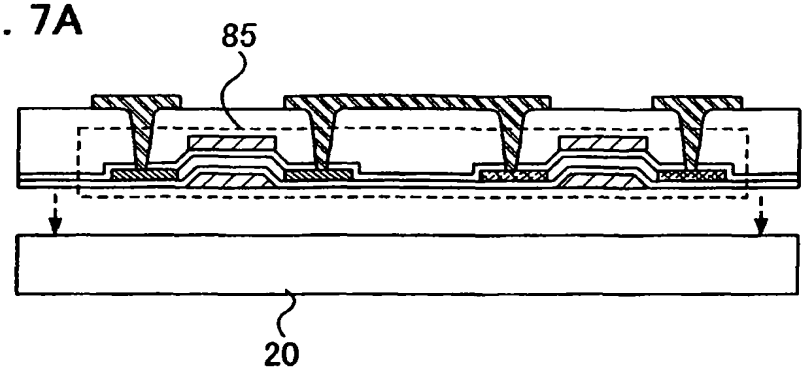


FIG. 7B

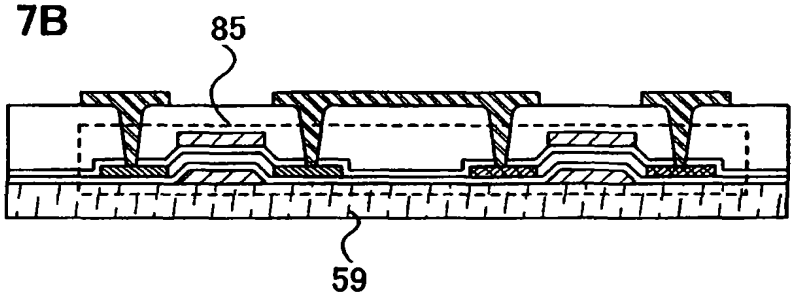


FIG. 7C

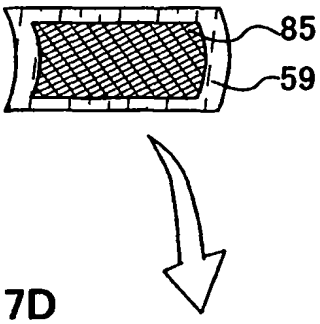


FIG. 7D

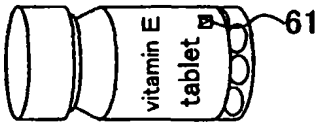


FIG. 8A

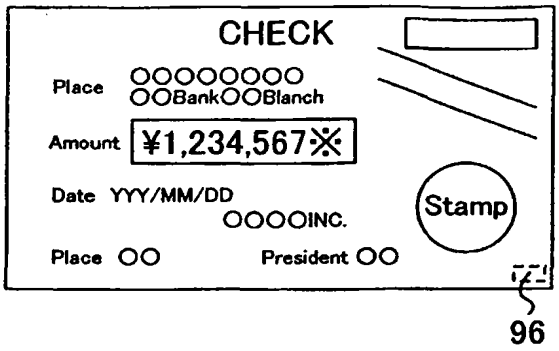


FIG. 8B

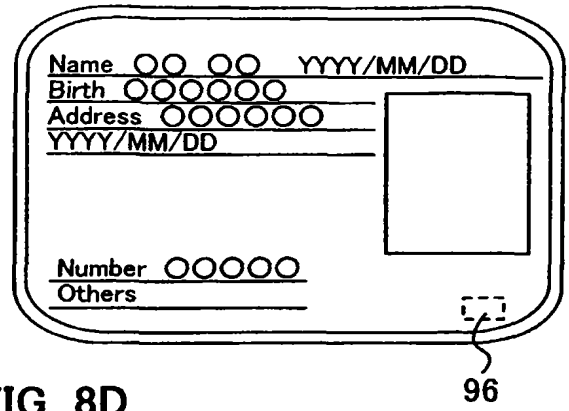


FIG. 8C

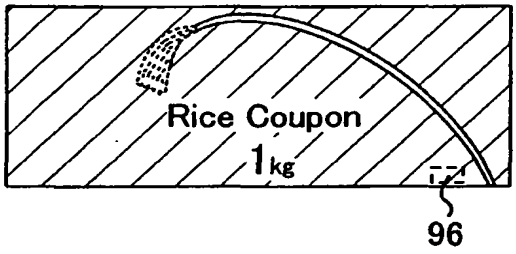


FIG. 8D

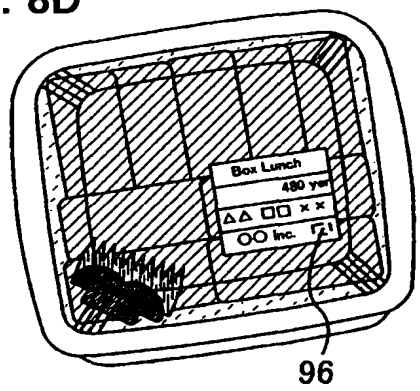


FIG. 8E

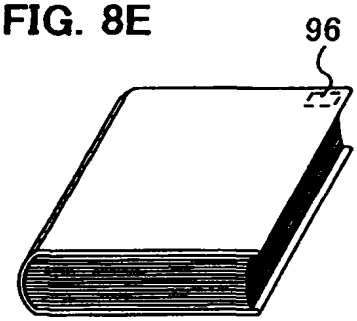


FIG. 8F

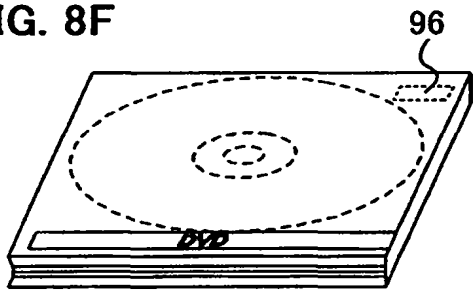


FIG. 8G

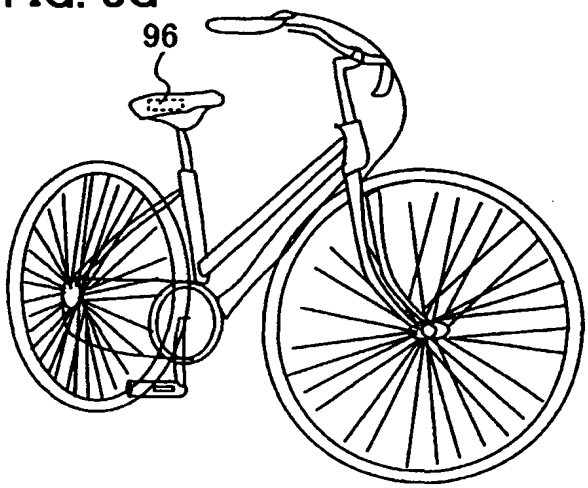


FIG. 8H

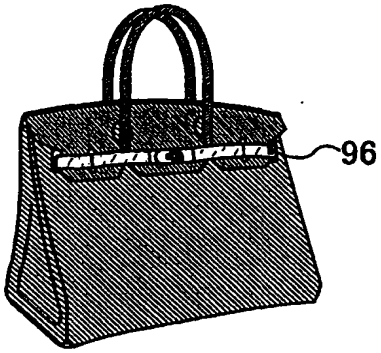


FIG. 9A

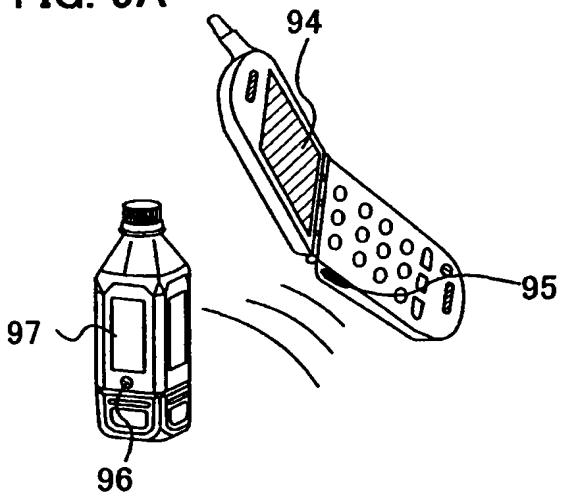


FIG. 9B

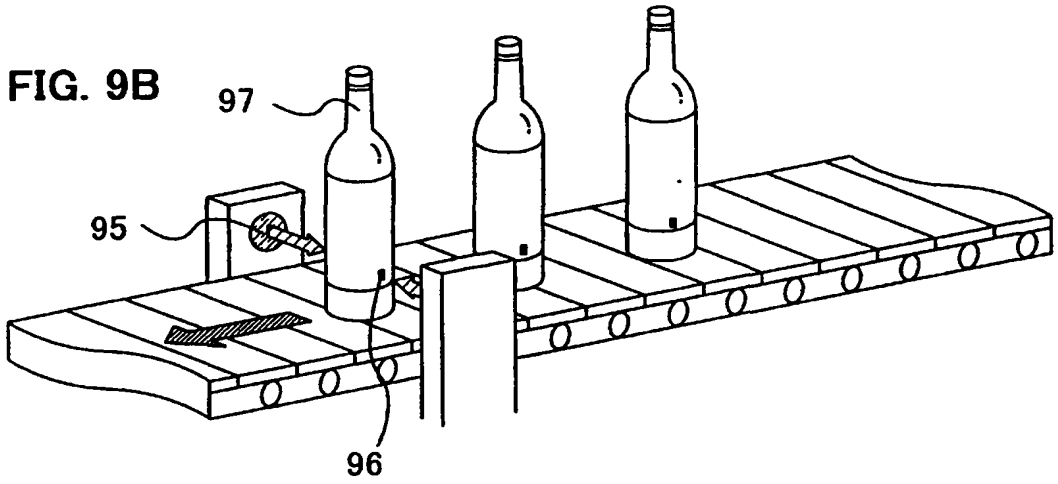


FIG. 10A

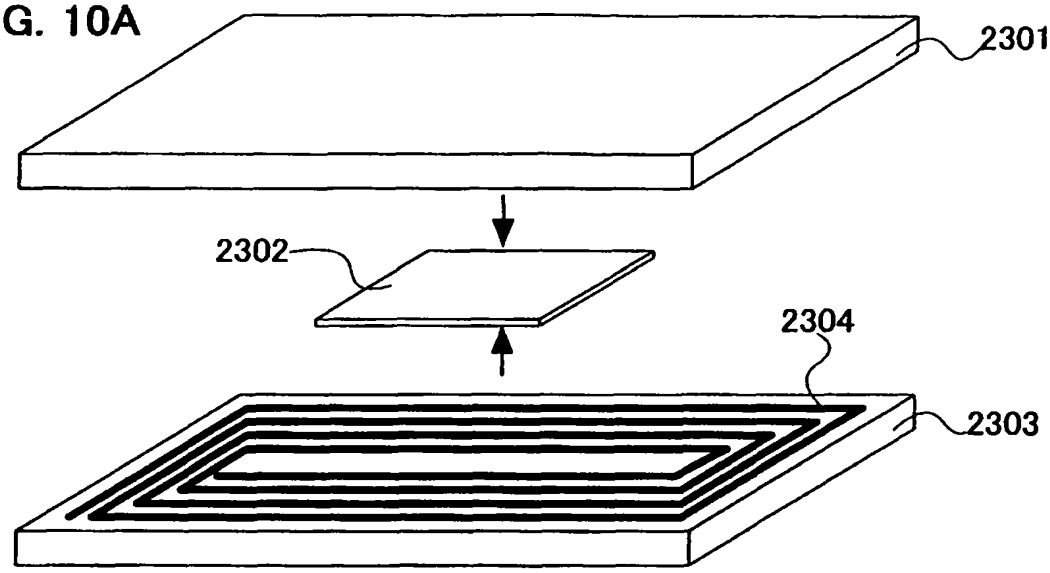


FIG. 10B

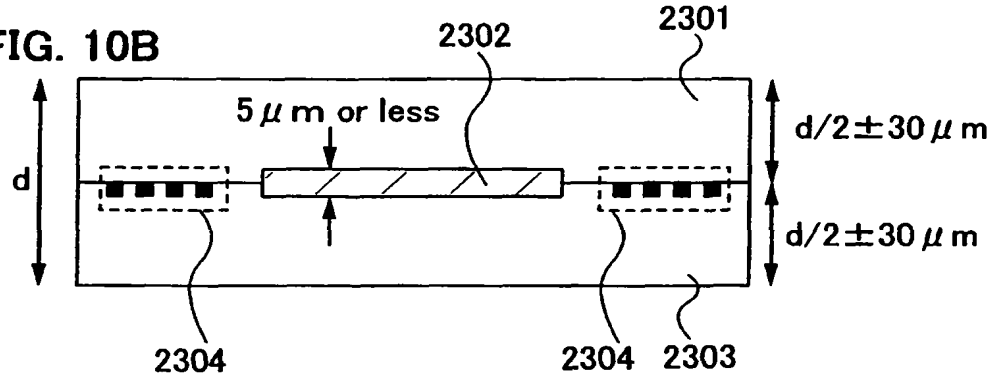
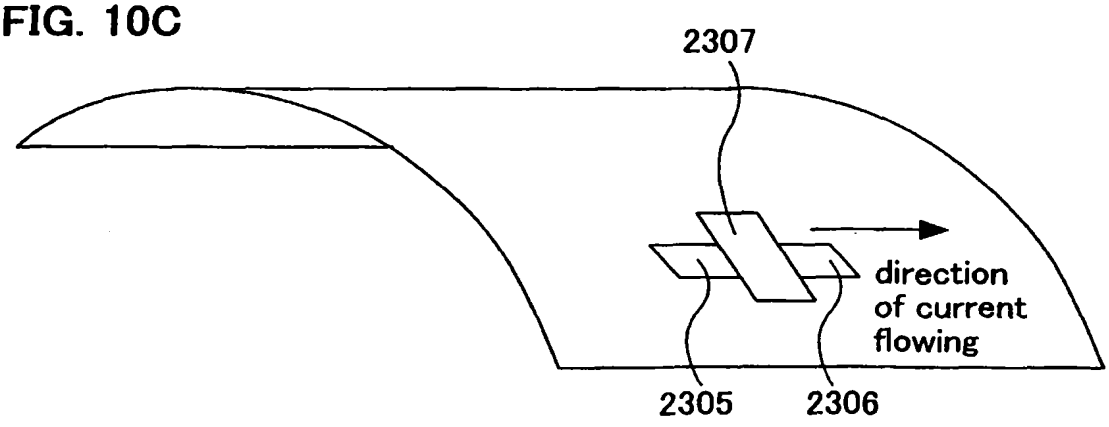


FIG. 10C



EXPLANATION OF REFERENCE

11: logic portion, 12: memory portion, 13: detecting portion, 14: Vth control, 15: antenna, 18: reader/writer, 20: substrate, 21: n-type transistor, 22: p-type transistor, 23: second gate electrode, 24: second gate electrode, 25: second gate insulating film, 26: source or drain region, 27: source or drain region, 28: source or drain region, 29: source or drain region, 30: channel forming region, 31: channel forming region, 32: first gate insulating film, 33: first gate electrode, 34: first gate electrode, 35: source or drain wiring, 36: source or drain wiring, 37: source or drain wiring, 51: timing control, 52: instruction decoder, 53: register array, 54: address logic and buffer, 55: data bus interface, 56: ALU, 57: instruction register, 59: substrate, 60: substrate, 61: wireless tag, 63: memory, 64: D/A converter portion, 65: buffer, 70: address bus, 71: address comparator, 72: address memory, 73: counter, 74: reset signal generating circuit, 75: discriminating circuit, 76: discriminating reference data memory, 77: EXOR circuit, 78: EXOR circuit, 79: EXOR circuit, 80: EXOR circuit, 81: NOR circuit, 82: latch circuit, 84: substrate, 85: element group, 86: terminal portion, 87: conductive particle, 88: resin, 91: curve, 92: curve, 93: curve, 94: display portion, 95: reader/writer, 96: wireless tag, 97: product, 2301: protective layer, 2302: element group, 2303: protective layer, 2304: antenna, 2305: drain electrode, 2306: source electrode, 2307: gate electrode